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Toward fast, low-noise charge-coupled devices for Lynx

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Abstract. Lynx requires large-format x-ray imaging detectors with performance at least as good as the best current-generation devices but with much higher readout rates. We are investigating an advanced charge-coupled device (CCD) detector architecture under development at MIT Lincoln Laboratory for use in the Lynx high-definition x-ray imager and x-ray grating spectrometer instruments. This architecture features a CMOS-compatible detector integrated with parallel CMOS signal processing chains. Fast, low-noise amplifiers and highly parallel signal processing provide the high frame rates required. CMOS-compatibility of the CCD enables low-power charge transfer and signal processing. We report on the performance of CMOS-compatible test CCDs read at pixel rates up to 5.0 Mpix s^{-1} (50 times faster than Chandra ACIS CCDs), with transfer clock swings as low as 1.0-V peak-to-peak (power/gate-area comparable to ACIS CCDs at 100 times the parallel transfer rate). We measure read noise of 4.6 electrons RMS at 2.5 MHz and x-ray spectral resolution better than 150-eV full-width at half maximum at 5.9 keV for single-pixel events. We report charge transfer efficiency measurements and demonstrate that buried channel trough implants as narrow as 0.8 μm are effective in improving charge transfer performance. We find that the charge transfer efficiency of these devices drops significantly as detector temperature is reduced from ~ -30°C to -60°C. We point out the potential of previously demonstrated curved-detector fabrication technology for simplifying the design of the Lynx high-definition imager. We discuss the expected detector radiation tolerance at these relatively high transfer rates. Finally, we note that the high pixel "aspect ratio" (depletion depth: pixel size $\approx 9:1$) of our test devices is similar to that expected for Lynx detectors and discuss implications of this geometry for x-ray performance and noise requirements. © *The Authors. Published by SPIE under a Creative Commons Attribution 4.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI.* [DOI: 10.1117/1.JATIS.5.2.021015]

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1 Introduction

Nearly two decades after the launch of Chandra and XMM/Newton, a new generation of large, scientifically ambitious, and exciting x-ray astrophysics missions is being planned. Athena, the European Space Agency's second L-class mission, will probe the physics of large-scale cosmic structures, trace the evolution of supermassive black holes, and explore the astrophysics of high-energy events ranging from stellar flares to supernova explosions.[1] Lynx, one of four large mission concepts being studied by NASA, aims to find and understand the origin of the very first supermassive black holes, explain just how the evolution of galaxies influences and is shaped by the hot, diffuse gas that surrounds them, and probe in unprecedented depth the high-energy processes that accompany stellar birth and death.[2]

Inspired by some of the most fundamental questions raised by their predecessors, these new missions require significant technical progress in optics and instruments. For example, Lynx requires effective area $\approx 30\times$ that of Chandra with half-arcsecond angular resolution, and an x-ray microcalorimeter with several thousand times as many pixels, and at several times better energy resolution, than was provided by the Hitomi soft x-ray spectrometer.[3]

Lynx also requires a $\sim$16-megapixel imaging instrument, the high-definition x-ray imager[4] (HDXI) with a field of view of several hundred square arcminutes. A brief summary of HDXI requirements is presented in Table 1. Although at first glance these requirements may not appear to be much more demanding than those of instruments already flown, in fact the very large throughput of the Lynx optics, coupled with the paramount importance of soft x-ray sensitivity to detect high-redshift sources, present formidable challenges for the HDXI sensor system. Significant technology development is needed to meet these requirements.

As discussed in Ref. 4 and elsewhere in this special issue, several sensor technologies now in development hold promise for Lynx HDXI. Active pixel sensors, which incorporate active circuit elements in each pixel, offer some attractive potential capabilities for this application. A particular implementation of this architecture, the depleted field effect transistor (DEPFET) sensor is being developed for the ATHENA wide-field imager (WFI) instrument and has demonstrated excellent performance.[5] Another approach, exploiting silicon-on-insulator technology, is being developed for the FORCE hard x-ray imaging mission.[6] Given the unique HDXI requirements for small pixels to sample the high-resolution Lynx optics (16 μm versus 130 μm for ATHENA WFI) and excellent low-energy response to study both highly redshifted and very soft cosmic sources (as low as 0.3 versus 1.0 keV for FORCE), two alternative architectures

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Table 1 Selected Lynx HDXI requirements.

Parameter	Value	Remarks
Primary science requirements		
Energy range	0.2 to 10 keV	
Field of view	$22' \times 22'$	PSF better than 1″ HPD over 10′ radius field
Spatial resolution	0.33″	16 μm ($F = 10$ m)
Spectral resolution	70-eV FWHM at 1 keV	
Derived requirements		
Read noise	Four electrons RMS	
Count-rate capability	8000 ct s^{-1}	Full field
Frame rate	100 frames s^{-1}	Full Field
	10^4 windows s^{-1}	~20″ × 20″ window

featuring readout circuitry in each pixel are being developed to meet HDXI requirements.[7,8]

The detectors developed for the HDXI may also serve in the readout subsystem of the Lynx x-ray grating spectrograph (XGS) instrument. As noted elsewhere in this special issue, XGS sensor requirements in the soft x-ray band (below ~2 keV) are similar to those of HDXI, and the detector technology we describe here has application in both instruments.

In this paper, we describe an advanced charge-coupled device (CCD) technology we are developing in part to meet the requirements of the Lynx HDXI and XGS. This "digital CCD" (DCCD) technology aims to provide the proven spectroscopic performance of conventional x-ray CCD detectors in a CMOS-compatible sensor capable of much higher frame rates with much lower power consumption. A recent overview of the objectives of this development program and our characterization of a first-generation test sensor have been presented elsewhere.[9] After a brief review of these results, we present performance data on a more capable second-generation sensor. We then sketch how this technology might be implemented in HDXI. As part of this discussion, we point out that use of well-developed curved detector technology might improve and simplify the HDXI sensor configuration. We note the challenges posed to any silicon detector technology in providing both the excellent low-energy x-ray response and the fine spatial resolution required by HDXI and XGS and identify some potential advantages of CCDs relative to APS in meeting these. We conclude with a summary and discussion of our near-term development plans.

2 Digital CCDs

2.1 *Overview*

MIT Lincoln Laboratory is developing technology to produce large-format visible imagers with the sensitivity, dynamic range, and uniformity of a scientific-grade CCD, integrated with the digitization and processing capabilities of a CMOS imager, and noise performance exceeding both image sensor types. We believe this program also holds great promise for high-energy astrophysics. The effort is proceeding along two parallel paths. The first aims to demonstrate a scientific grade analog CCD sensor with novel, high-speed (up to 5 MHz), low-noise (potentially subelectron per read) amplifiers, fabricated in a low-voltage CCD process allowing operation with voltages compatible with CMOS logic levels. The second path aims to develop compact, highly parallel signal processing chains allowing high frame rates with modest analog-to-digital conversion rates. When fully demonstrated, these two technologies will be combined, first as discrete elements, and then potentially as a single-detector module by means, for example, of three-dimensional integration of analog and digital tiers through hybrid wafer bonding. In principle, either of these configurations could be deployed in a flight instrument for Lynx.

This technology clearly offers great potential for Lynx. The fast, low-noise amplifiers and parallel architecture of the final product will provide the frame rate and noise performance required by the Lynx HDXI and XGS. CCD operation with CMOS-compatible clock voltages is critical for satisfying the size, mass, and power consumption constraints of a flight instrument. Here we report recent progress toward these goals.

2.2 *High-Speed, On-Chip Amplifiers*

High-speed p-channel JFET outputs have been the primary choice for most recent Lincoln CCD designs. This amplifier, depicted in Fig. 1(a), has a pJFET-based first-stage source follower with a second-stage nMOSFET buffer for added bandwidth. This circuit has been extensively used in small, high-frame-rate imagers for adaptive optics programs and has been implemented on the first DCCD run. Its responsivity is about twice that of the nMOSFET amplifier used on previous Lincoln designs used on Chandra and Suzaku, and the second stage enables up to 10-MHz pixel rates. Its superior noise performance is illustrated in Fig. 2.

A recently developed amplifier, called SiSeRO (single-electron sensitive readout), is illustrated in Fig. 1(b). This amplifier draws on earlier work on floating-gate amplifiers which demonstrated extremely high responsivity (200 μV/e−) and subelectron noise.[10] Here the charge packet is transferred beneath a p-channel MOSFET that is built atop the CCD channel. The image charge of the electrons in the pMOSFET channel modulates the transistor's drain current to produce an output signal. This amplifier almost eliminates parasitic capacitances (thereby boosting responsivity) and, because it nondestructively samples the charge packet, is not subject to reset noise as the pJFET is. This has important advantages for noise and signal processing circuitry. Moreover, even with the very high responsivity of the SiSeRO, a typical flight signal chain dynamic range would accommodate signals in excess of 9000 electrons (more than 30 keV), providing accurate spectroscopy of cosmic x-rays throughout the Lynx passband as well as clear discrimination between those x-rays and the minimum ionizing charged-particle background. We note that the SiSeRO architecture is similar in some respects to that of the very successful DEPFET developed for the Athena wide-field imager.[5]

Several versions of the SiSeRO amplifier incorporating design approaches were placed on the DCCD detectors described here. These devices are now under test, but performance has not yet

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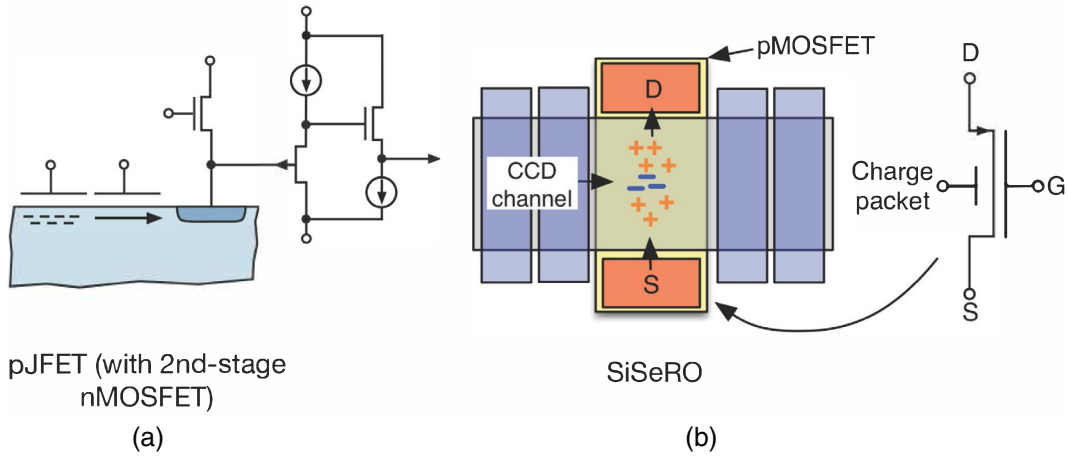

Fig. 1 Charge conversion amplifiers used in MIT/LL CCDs: (a) pJFET based on nMOSFET buffer in current use and (b) SiSeRO with floating-gate. Here the signal charge packet, represented by the "–" symbols, has been transferred along the CCD output register until it arrives under the p-channel MOSFET output transistor. In this position, which is effectively a back-gate for the pMOSFET, the signal charge modulates the transistor's drain current, represented by the "+" symbols.

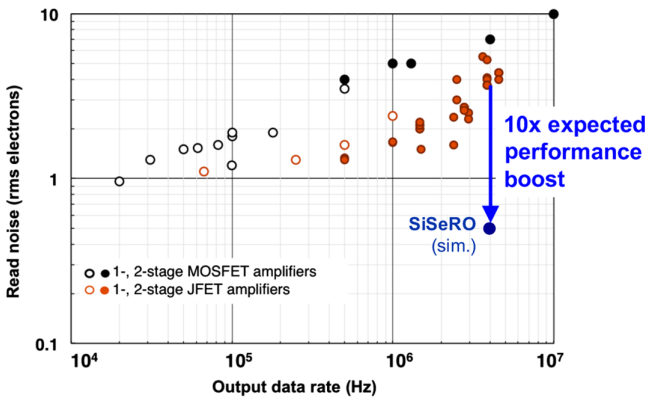

Fig. 2 Measured or calculated noise performance of various CCD amplifiers. Chandra and Suzaku devices have MOSFET amplifiers (measured noise plotted with open black circles) and operate at ≤100 kHz. Two-stage pJFETs in current use (measured noise plotted with filled red circles) show much lower noise at pixel rates ≥1 MHz. The SiSeRO amplifier is now in development, with goals of very high responsivity and subelectron noise at megahertz pixel rates.

been optimized. We defer further discussion of the SiSeRO amplifier to future work.

2.3 *Single-Level Polysilicon Transfer Gates*

A key element of the DCCD program enabling low-power, high-speed CCD operation is the implementation of single-level polysilicon process to form all of the CCD gate electrodes. This technology exploits deep-submicron (193/248-nm wavelength) lithography and plasma etching to achieve isolation between phases, along with scaled dielectric thickness and implant dose/energies to maintain sensor performance while allowing operation at significantly reduced voltages.[11,12] Compared to conventional multipoly fabrication, single-poly technology requires fewer fabrication steps, enables better control of dopant diffusion, and results in fewer defects. Moreover, experience shows that the single-poly process achieves greater uniformity

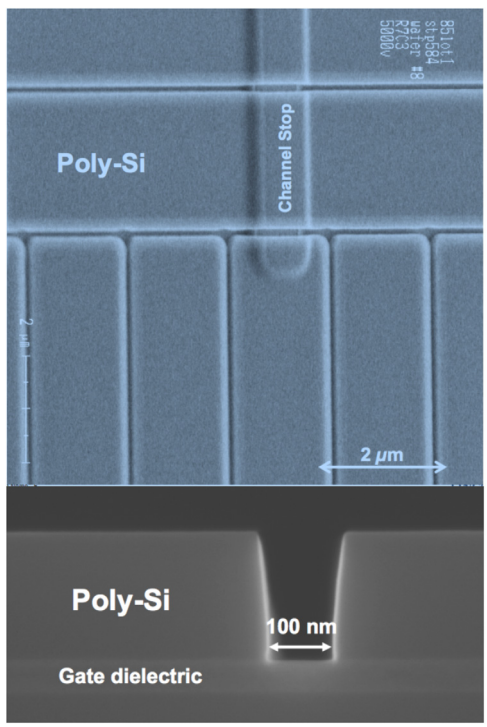

Fig. 3 Scanning electron micrograph images of single polysilicon electrode CCDs mix-and-match patterned with 193-/248-nm lithography on 200-mm wafers. (a) Parallel to serial register transition and (b) cross section.

in threshold voltage and more reliable charge transfer with fixed, CMOS-compatible clock swings. The lower-amplitude clocks can be controlled with CMOS circuitry and yield substantial savings in clock power consumption, which varies as the square of the clock amplitude. The SEM photos in Fig. 3 show the gate structure of the first devices produced for the DCCD program on 200-mm wafers. In addition to the test devices we discuss here, large format (2k × 1k, 24-μm pixel) frame-transfer imagers have been successfully produced with this process.

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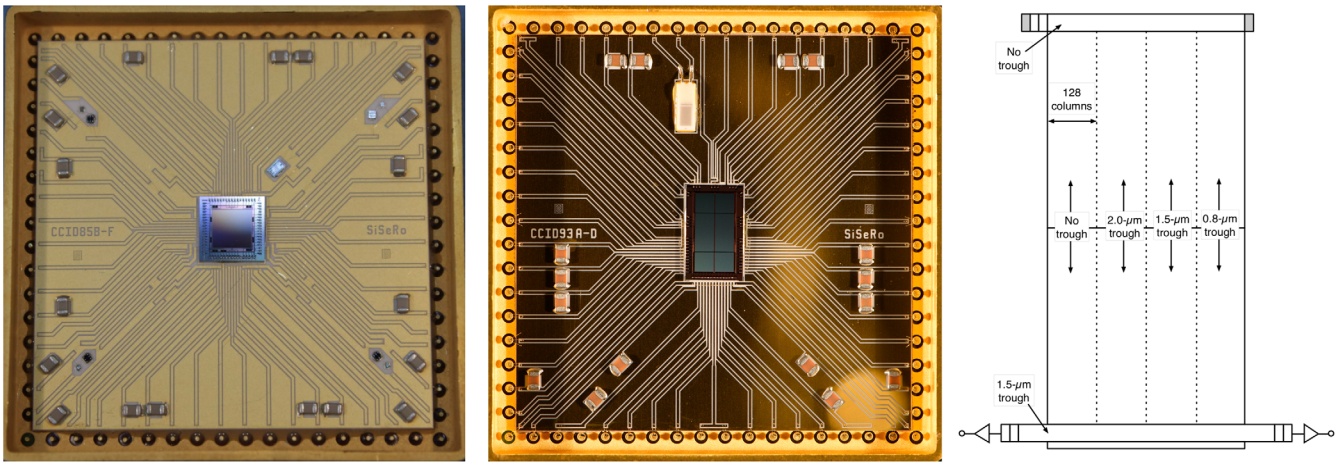

(a) (b) (c)

Fig. 4 (a) CCID85 and (b) CCID93 test devices. The active areas of the CCID85 and CCID93 are 4×4 mm and 4×8 mm, respectively; the test packages are approximately 48 mm^2. (c) Layout of the CCID93. The four segments of the device are equipped with buried channel trough implants of different widths.

2.4 *Test Devices*

We report here the performance of two different DCCD test arrays, illustrated in Fig. 4. A first-generation device, designated CCID85, was designed to test readout amplifier architectures and to evaluate low-voltage, CMOS-compatible CCD technology. It has a 512×512 array of 8-μm pixels with amplifiers on all four corners. Amplifier variations include the pJFET and low-speed versions of the SiSeRO amplifier. The CCID85 features substrate bias independent of charge-transfer gates for deep-depletion, allowing for thick, back-illuminated devices. At present, only front-illuminated versions have been produced.

A second-generation device, designated CCID93, has been designed to continue amplifier development and to evaluate radiation tolerance in a frame-transfer architecture. It is twice the size of the CCID85, with 512×512 arrays of 8-μm pixels in both the imaging and framestore areas. The CCID93 has two amplifiers at opposite ends of its bidirectional output register. One is a modified version of the pJFET output used on the CCID85, and the other is a two-stage implementation of the SiSeRO designed for higher readout rates. The CCID93 includes a number of features for enhanced radiation tolerance, including a charge injection register and buried channel trough implants[13] of several different widths, as illustrated in Fig. 4(c). X-ray performance characteristics of a front-illuminated CCID93 are described in this paper. Performance and radiation tolerance of a back-illuminated version now in fabrication will be reported elsewhere.

The CCID85 and the CCID93 devices we tested were fabricated in MIT Lincoln Laboratory's Microelectronics Laboratory on p-type float zone silicon of at least 3000 ohm-cm resistivity. Both devices are equipped with a substrate bias connection, which provides substantial depletion layer thickness even with CMOS-compatible gate voltages. With the substrate biased to -5 V, we measured a depletion layer thickness of approximately 75 μm in these devices using a technique we developed previously.[14] The results reported in the following sections were obtained with this substrate bias.

2.5 *Test Results: CCID85*

As we reported previously,[9] we have operated the first-generation CCID85 test devices via pJFET outputs at pixel rates ranging from 1.25 to 5 MHz, with parallel registers clocked during readout at 200 kHz. Including 50 "overclocked" pixels per row, the frame readout time at 2.5 MHz is 118 ms. To obtain the data reported here we cooled the device to -49°C and acquired a series of images, integrating for 500 ms between the end of one readout and the start of the next. Data were obtained at the MIT Kavli Institute (MKI) using a Lincoln Laboratory-developed test system comprising readout electronics integrated with a thermoelectrically cooled vacuum cryostat.

A representative x-ray spectrum obtained with a radioactive ^{55}Fe source is shown in Fig. 5. Device performance is summarized in Table 2. We measure system (CCD and laboratory

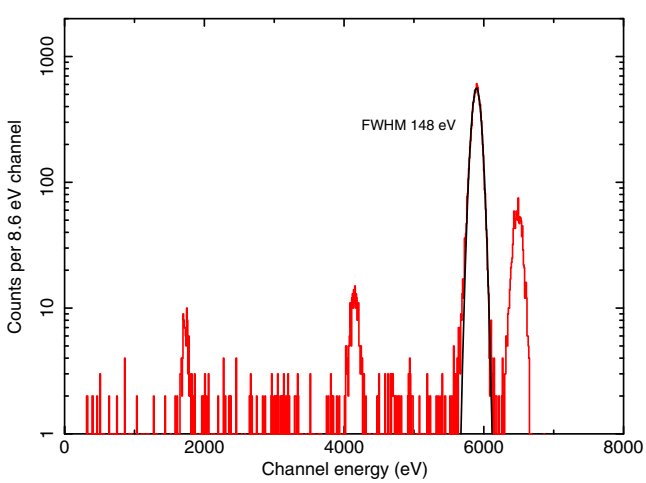

Fig. 5 Single-pixel x-ray event spectrum obtained with the CCID85 test device read at 2.5-MHz and exposed to a radioactive ^{55}Fe source. The red histogram shows measured data; the black curve shows a Gaussian fit to the Mn Kα peak at 5895 eV. The FWHM of the best-fit model is 148 eV. Mn Kβ (at 6490 eV) as well as Si K-escape (at 4100 eV) and fluorescence peaks (at 1740 eV) are also visible.

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Table 2 Measured performance and operating conditions of first-generation CCID85.

Parameter	Value	Remarks
Operating conditions		
Pixel rate	1.25 to 5 MHz	
Clock levels (parallel and serial)	−1.5 to +3 V (typical) −1.5 to +1.5 V (CTI measurements)	±1.5 V is minimum swing allowed by lab electronics
Detector temperature	−49°C	
Measured performance with pJFET amplifier		
Responsivity	21 μV per electron	
System read noise	6.5 to 7.2 electrons RMS at 2.5 MHz 10 electrons RMS at 5 MHz	Includes lab electronics noise of 3.3 electrons RMS
Inferred pJFET read noise	5.5 to 6.4 electrons RMS at 2.5 MHz 9.4 electrons RMS at 5 MHz	Excluding lab electronics noise
Spectral resolution	148- to 151-eV FWHM at 5.9 keV	Single-pixel events
CTI	Parallel: $(3.7 \pm 1.2) \times 10^{-6}$ per transfer Serial: $<0.8 \times 10^{-6}$ per transfer	At 5.9 keV; 90% confidence
Dark current	2.0 electrons per pixel per second	At −49°C

electronics combined) noise levels in the range of 6.5 to 7.2 electrons RMS at 2.5 MHz and single-pixel x-ray event spectral resolution for 145 to 150 eV full-width at half-maximum (FWHM) at 5.9 keV. (A single-pixel event is one for which the signal in each of the eight nearest-neighbor pixels is no greater than a "split threshold," in this case set at 20 electrons.) Responsivity, as expected, is higher than that observed with previous generation MOSFET amplifiers. Charge transfer inefficiency (CTI), though not tightly constrained in this relatively small device, is good. In fact, we can provide only an upper limit on the CTI of the serial register when operated at 2.5 MHz with 2.7-V peak-to-peak clock swings. Both CTI and dark current are sufficiently low that they do not compromise x-ray spectral resolution.

2.6 *Test Results: CCID93*

Here we present the first test results from the CCID93. We tested one of these devices at the wafer level at MIT Lincoln Laboratory and a second one in packaged form at MKI. The wafer level test environment enables rapid screening for device functionality and operating point optimization. The MKI characterization employed an improved, lower-noise version of the test system used for the CCID85 equipped with a revised cryostat capable of reaching lower detector operating temperatures. In this section, we first present CCID93 amplifier performance and x-ray spectral resolution measurements obtained at MKI and then discuss charge transfer performance measurements obtained at both Lincoln and MKI.

2.6.1 *CCID93 amplifier performance and x-ray spectral resolution*

We used our revised test system to read a CCID93 via its pJFET output at pixels rates of 1.25 and 2.5 MHz, with the parallel registers clocked at 0.2 MHz. Including the eight extended pixels in the output register and 42 "overclocked" pixels per row, the frame readout time at 2.5 MHz is 235 ms. For all results reported here, the entire device (image area and framestore) was exposed and read for each frame. As with the CCID85, we acquired a series of images, integrating for 500 ms between the end of one readout and the start of the next. We obtained data with detector temperatures ranging from −26°C to −58°C.

A representative x-ray spectrum obtained with an ^{55}Fe x-ray source is shown in Fig. 6. Device performance is summarized in Table 3.

We measure a system noise level of 4.6 electrons RMS at 2.5 MHz. The estimated electronics noise contribution to this measurement (less than one electron, RMS) is negligible. The CCID93 pJFET noise performance is thus significantly better than the CCID85's 6 electrons RMS for the detector alone (see Table 2). The measured responsivity of the CCID93 pJFET, at 35 μV per electron, is higher than that of the CCID85 by a factor of nearly 1.7. We attribute these improvements to several design changes in the CCID93's output amplifier.

The best Mn Kα line width we measure (145-eV FWHM at −26°C, for single-pixel events (here a split threshold of 24 electrons is used to select single-pixel events), is broader than we can account for given our measurements of readout noise, dark current, and CTI alone. These contributions are itemized in Table 4. The magnitude of the discrepancy is equivalent to an additional 50-eV FWHM or a noise source of 5.8 electrons, RMS. A likely mechanism for this additional noise is random variation in the amount of signal-charge lost to adjacent pixels.

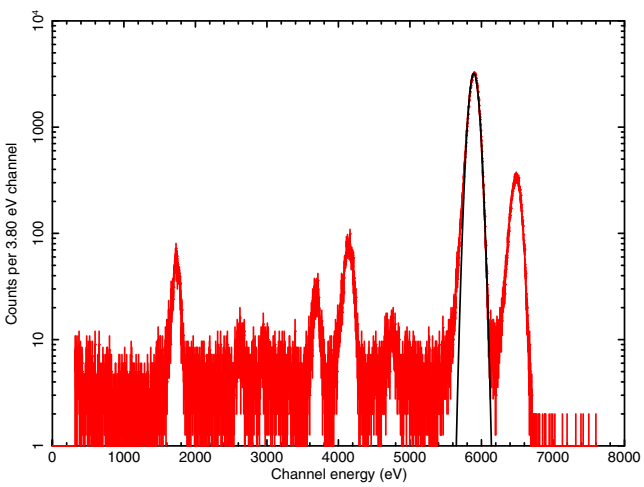

Fig. 6 Single-pixel x-ray event spectrum obtained with the CCID93 test device read at 2.5 MHz and exposed to a radioactive ^{55}Fe source. The red histogram shows measured data; the black curve shows a Gaussian fit to the Mn Kα peak at 5895 eV. The FWHM of the best-fit model is 147 eV. Mn Kβ (at 6490 eV), Si K-escape (at 4100 eV), and fluorescence peaks (at 1740 eV) are visible, as are other lines characteristic of materials in the test cryostat.

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Table 3 Operating parameters and performance of the CCID93. Note that spectral resolution and CTI values are quoted for the device region with a 1.5-μm-wide trough. See Sec. 2.6.2.

Parameter	Value	Remarks
Operating conditions		
Clock rates	Serial: 1.25 to 2.5 MHz Parallel: 0.2 MHz	Some CTI measurements at 1-MHz parallel rate
Clock levels	Serial: −2.0 to +2.0 V Parallel: −1.35 to +1.35 V	Some CTI measurements at ±0.5 to ±1.5 V parallel
Detector temperature	−26°C to −58°C	
Measured performance with pJFET amplifier		
Responsivity	35 μV per electron	
System read noise	4.6 electrons RMS at 2.5 MHz	Includes lab electronics noise
Spectral resolution at 5.9 keV	145- to 148-eV FWHM ($T = -26$°C) 155- to 157-eV FWHM ($T = -58$°C)	Single-pixel events Split-event threshold 24 electrons
CTI		
Parallel	$(8.1 \pm 0.37) \times 10^{-6}$ ($T = -26$°C) $(1.8 \pm 0.07) \times 10^{-5}$ ($T = -58$°C)	±1.35 V par. clock amplitude
Serial	$(-0.1 \pm 1.7) \times 10^{-6}$ ($T = -26$°C) $(6.1 \pm 2.1) \times 10^{-6}$ ($T = -58$°C)	$<3.3 \times 10^{-6}$ at 95% confidence
Full well capacity	>12,500 electrons	−4.0 to −2.0 V par. clock amplitude
Dark current	1.2 e^- pixel^{-1} s^{-1} ($T = -50$°C)	

Table 4 Contributions to single-pixel event spectral resolution at 5.9 keV. The measured line width exceeds the total attributable to the components listed here.

Component	FWHM (eV)	Remarks
Fano noise at 5895 eV	117	$F = 0.115$; $w = 3.65$ eV/e^-
Read noise	40	4.6e^-, single read
Dark current	29	12.4e^- per pixel $T = -26$°C
CTI	49	8.1×10^{-6}; 1024 transfers
Total	136	RSS

As noted above, by selection, pixels neighboring a single-pixel x-ray event can contain charge no greater than the "split-event" threshold, which is set at a multiple of the measured total (readout plus dark current) noise and is typically 20 to 25 electrons.

We performed a preliminary analysis of the spatial distribution of charge in single-pixel events, fitting a circularly symmetric, two-dimensional Gaussian to each event. Characteristic (two-dimensional) standard deviations range from 1.6 to 3.2 μm, suggesting that a significant proportion of single-pixel events have indeed shared some (subthreshold) signal charge to adjacent pixels, and that the charge sharing process is a very plausible explanation for the spectral width we measure.

A more quantitative analysis of this process is beyond the scope of this paper. Here we note that, despite the larger pixel size of the HDXI, charge sharing will be a significant contributor to its spectral resolution budget, given its large depletion depth (100 μm versus an estimated 75 μm for our test devices) and back-illuminated configuration. This conclusion is relevant to any silicon detector technology. We return to this point in Sec. 3.3.

X-ray interactions for which a large fraction of charge is not collected in a central 3×3 pixel neighborhood produce the so-called "partial event floor," visible in Fig. 6 as a nearly flat spectral feature extending from the Mn K peaks to the lowest energies. These events may be produced by x-rays absorbed in the undepleted silicon below the depletion region in this front-illuminated device. Charge from these events will experience significantly more lateral diffusion than events produced in the depleted silicon. Such events may also suffer appreciable charge loss to the undepleted bulk. We quantified the partial event floor by fitting a model to the data in Fig. 6. The model consists of a constant component representing the floor plus a series of Gaussian peaks. The fit yields a floor level of 4.0 ± 0.1 counts per 3.8 eV spectral channel. Integrated from 500 eV to 6.4 keV, the partial event floor contains about 0.7% of the detected events. The average amplitude density (mean counts per spectral bin) of the floor is about 0.11% of the maximum amplitude of the Mn Kα feature. We note that the floor amplitude depends on the value of the split-event threshold parameter used to select single-pixel events. We expect that the floor amplitude will be different for the fully depleted back-illuminated device we plan to test in the near future.

The single-pixel-event x-ray resolution depends on detector temperature. We measure 145 to 148 eV (FWHM) at 5.9 keV at −26°C and 155 to 157 eV at −58°C. We attribute the difference in resolution to the temperature dependence of the CTI, as discussed in Sec. 2.6.2. We note that the increased CTI more than compensates for the reduced dark current at −58°C.

As shown in Table 3, even at a relatively low parallel clock swing of 2-V peak-to-peak, the full well capacity of the CCID93 is more than adequate for x-ray imaging spectroscopy applications in the Lynx band. This capacity exceeds both the charge deposited by the most energetic cosmic x-rays focused by the Lynx optics (~10 keV ≈ 2700 electrons), and the nominal median charge deposited by a minimum ionizing charged particle traversing the 100-μm depletion depth in a single HDXI pixel (~8000 electrons). Although in practice an HDXI signal chain is likely to saturate before the sensor's full well capacity is reached, there is ample dynamic range to discriminate in-band x-ray signals from such large charged particle signals. We note also that an HDXI sensor would likely feature 16-μm pixels (see

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Table 1 and Sec. 3.3). For a trough of a given width, this would provide roughly twice the full well capacity of the CCID93's 8-μm pixels.

2.6.2 *CCID93 charge transfer performance*

Charge transfer efficiency, the fraction of a charge in a packet successfully transferred from one CCD shift register element to the next, is a critical x-ray CCD performance parameter. It is well-known that charge transfer efficiency depends on many factors, including device architecture, fabrication processes, and charge transfer clock speed and amplitude. It is, therefore, important to characterize the charge transfer efficiency of our CMOS compatible, single-level polysilicon CCDs operating at high transfer rates and low clock amplitudes. The architecture and larger format of the CCID93 allow us to do so, and here we present initial results of an ongoing study. We express our results in terms of CTI, which is the mathematical complement of charge transfer efficiency.

We use monochromatic x-ray illumination by a radioactive ^{55}Fe source to measure CTI of CCID93 devices as a function of clock rate, amplitude, and detector temperature. CTI can in principle be measured for both the parallel ("vertical") registers and the serial ("output" or "horizontal") register. As noted above in Sec. 2.4, the parallel registers of the CCID93 contain buried channel trough implants of various widths to improve CTI and radiation tolerance. We are, therefore, also able to characterize CTI as a function of trough width. As we discuss below, this feature does complicate the measurement of serial CTI in this device.

Our CTI measurement method is illustrated in Fig. 7, which shows how data are used to determine parallel CTI for one sector of the CCID93. Briefly, well-collected x-ray events are identified and their amplitudes are measured as a function of event position in the image. The variation of x-ray signal amplitude with array position is used to measure CTI. The data in Fig. 7 were obtained at the Lincoln Laboratory probe station with a parallel clock rate of 1 MHz (100 times that used for Chandra ACIS CCDs) from a CCID93 segment equipped with 1.5-μm wide troughs. The detector temperature was −30°C. This figure shows that for this trough width and clock rate, charge transfer is better (CTI is lower) at the higher parallel clock swing.

Figure 8(a) shows the variation of parallel CTI with trough width for two temperatures. These data were obtained at a parallel clock swing of 2.7 V (peak-to-peak), parallel clock rate of 0.2 MHz, and serial clock rate of 2.5 MHz with the detector at temperatures of −26°C and −58°C. In this figure, the data obtained from the trough-free region of the device are plotted at a transfer channel width of 7 μm, as this is the distance between adjacent (1-μm-wide) channel stops. Under these conditions, the additional trough implant (transfer channel widths 0.8 to 2.0 in this figure) clearly improves (lowers) the CTI. Note, however, that CTI is almost independent of trough width. The CTI is clearly worse (higher) at the lower detector temperature for all trough configurations.

Figure 8(b) shows the variation of parallel CTI with parallel clock swing at the higher clock rate of 1 MHz and lower serial rate of 0.5 MHz. Two trough configurations (no trough and 2.0-μm-wide trough) are shown; the detector temperature is −30°C. Under these conditions, the presence of the trough is also seen to improve CTI. For the 2.0-μm-wide trough, the CTI is roughly independent of clock swing down to the lowest swing measured (1-V peak-to-peak). In the absence of a trough, however, the CTI is independent of clock swing only for swings of at least 2-V peak-to-peak. At 1-V swing, the CTI in the no-trough region was so large that we found it difficult to measure reliably, so no CTI value is shown for that case.

Figure 9 explores the impact of trough width on parallel CTI and x-ray spectral resolution in greater detail. It presents single-pixel x-ray event spectra obtained from a packaged CCID93 operating in a low-noise test system at MKI and illuminated by an ^{55}Fe source. Figures 9(a) and (b) show spectra obtained

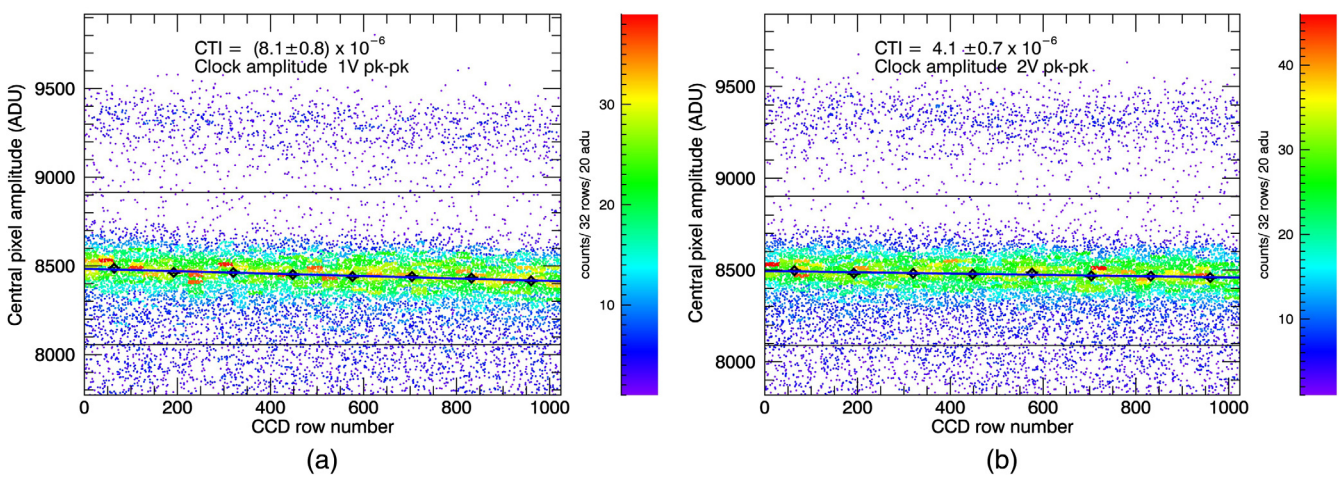

Fig. 7 Scatter plots of pixel amplitude as function of row obtained from x-ray illumination of a CCID93 detector at a temperature of −30°C. These plots illustrate parallel CTI at 1-MHz parallel clock and 0.5-MHz serial rate (1-ms row transfer period) for two values of clock amplitude. (a) Parallel clock swing 1-V peak-to-peak and (b) parallel clock swing 2-V peak-to-peak. A radioactive ^{55}Fe was used. The point locations show "center pixel" amplitude, in analog-to-digital converter units (1 ADU = 0.19 electrons) as function of row number, with color indicating the local density of events in the ADU-row plane. The large diamonds show the most probable pulse-height (within broad amplitude limits indicated by the thin black horizontal lines) in each of 8 128-row bins. Estimated uncertainties in the diamonds are of order 2 ADU. A linear fit to the diamonds (thick black line) provides a CTI estimate.

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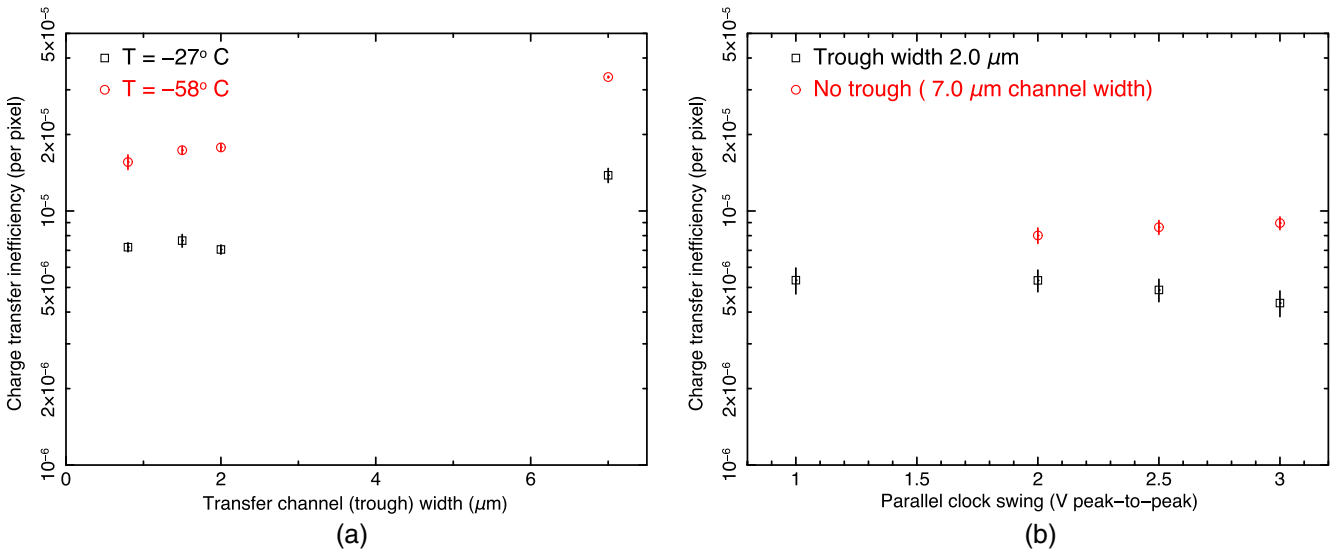

Fig. 8 CCID93 CTI: (a) CTI for each trough configuration at two detector temperatures. Data from the trough-free segment of the device are plotted at a transfer channel width of 7.0 μm, the distance between adjacent channel stops. Parallel clock rate of 0.2 MHz, serial clock rate of 2.5 MHz, and parallel clock swing of 2.7 V. (b) CTI dependence on parallel clock swing (peak-to-peak) for two trough configurations. Parallel clock rate of 1 MHz and serial clock rate of 0.5 MHz. The detector temperature was −30°C. For the no-trough configuration, CTI at 1-V swing is too large to measure reliably and is not shown.

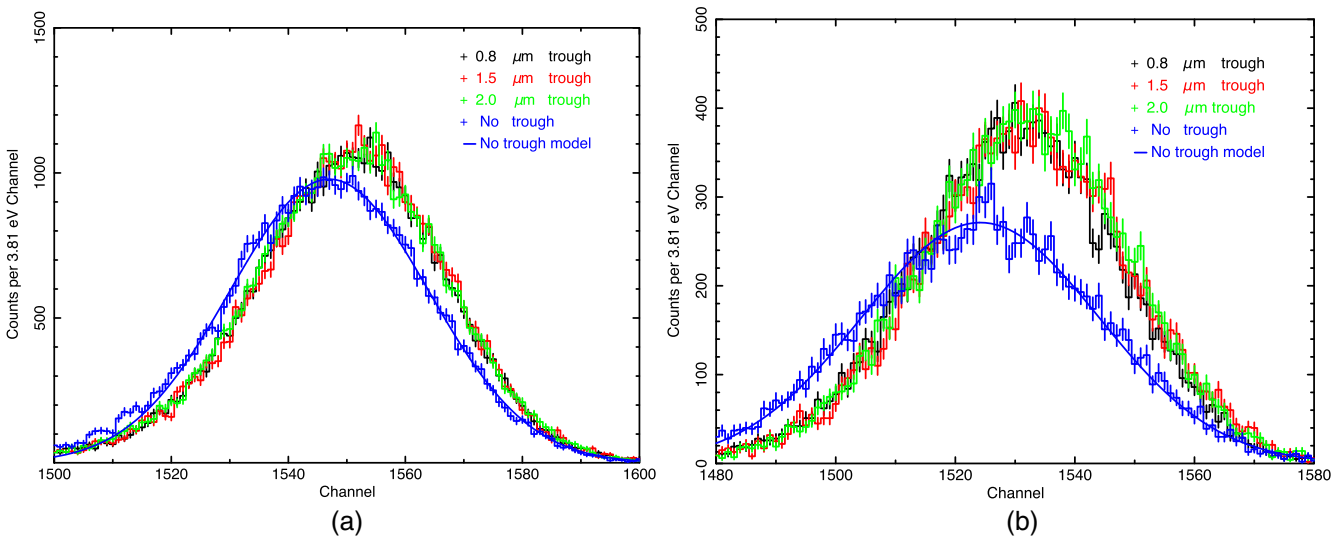

Fig. 9 The effect of CTI on single-pixel x-ray spectral resolution is illustrated. The detector response to the Mn Kα complex (5895 eV) is shown for two different detector temperatures [(a) −26°C and (b) −58°C] At a given temperature, the spectra obtained from the three different trough implant widths (0.8, 1.5, and 2.0 μm) are statistically identical. The peak from the region without a trough implant is clearly shifted to lower energy and broadened, indicating a larger CTI there. The smooth curve through the no-trough data is a best fit Gaussian model. The data were obtained with parallel clock rate of 0.2 MHz, serial clock rate of 2.5 MHz, and parallel clock swing of 2.7 V.

with the detector at temperatures of −26°C and −58°C, respectively. Each panel shows a distinct spectrum for each of the four trough configurations. At a given temperature, the spectra from the three detector segments with different trough implants are essentially indistinguishable, whereas the spectrum from the region with no trough implant is shifted to lower energy and broadened. With the detector at −26°C (a), the shift is 12.1 eV and the FWHM is broadened from 146 to 152 eV in the no-trough region. With the detector at −58°C (b), the CTI is roughly a factor of two higher, the shift is 25.2 eV, and the FWHM is broadened from 158 to 182 eV.

The serial register transfers charge packets that have already been transferred by a parallel register, so serial CTI measurements are affected by parallel CTI variations among the four device sectors. We therefore measure serial CTI separately for each sector. Since there are only 128 serial register elements serving each sector, however, these individual measurements are less precise than our parallel CTI measurements. Measured

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serial CTI in each sector is found to be consistent, within these relatively large errors, with the weighted mean value for all sectors. We report these weighted means in Table 3. At a detector temperature of −26°C, serial CTI is consistent with zero at the 95% confidence level. At a detector temperature −58°C, serial CTI is measured with marginal significance. We note that the serial register contains a trough 1.5-μm-wide, and that at both detector temperatures, serial CTI appears to be better (lower) than parallel CTI in parallel registers of the same trough width, as shown in Table 3.

We summarize our CTI results as follows. With trough implants, these devices show good charge transfer efficiency with parallel register clock rates as high as 1 MHz (100 times the rate of Chandra ACIS) and serial register clock rates of 2.5 MHz. These results were obtained with parallel clock amplitudes as low as 1-V peak-to-peak (one-tenth that of ACIS). With measured gate capacitance (about 7 to 8 $\mathrm{nF\,cm^{-2}}$ per phase) comparable to those of earlier triple-poly devices, these results suggest that HDXI frame rates can be achieved with clock power dissipation per unit area not very different from that required for much slower, legacy instruments, while clocking 100 times faster. We note that a two-phase version of the CCID93 we will soon test may require even lower transfer clock power.

At present, only top-level performance requirements for HDXI have been established, and these have not yet been flowed to lower level requirements on device parameters such as CTI. As noted in Sec. 3.1, the actual CTI requirement will depend on the size of individual detectors populating the HDXI focal surface. For the smaller, segmented CCD described there, the measured CTI of the CCID93 (with trough) is more than adequate, as at most 64 parallel transfers would be required for any given charge packet. For the larger, frame-transfer device concept, however, CTI of order 10^{-6} per pixel, for that device's 16-μm pixels, would be required. Although it is not straightforward to scale our CCID93 CTI measurements to the larger pixel size of the concept device, it is quite likely that some improvement in charge transfer performance will be required to meet this requirement. Further fabrication process adjustments, together with measurements of a device with 16-μm pixels, will likely be necessary to do so. We note that legacy (Chandra and Suzaku) devices have achieved CTI as low as 10^{-6} per 24-μm pixel.

Our finding that CTI is relatively insensitive to trough width may be evidence that all three of the CCID93 trough designs produce significant lateral fringing fields extending across the pixel (from channel stop to channel stop). These fields may confine relatively small x-ray-induced charge packets to channels of similar lateral extent. The effectiveness of the 0.8-μm-wide trough is especially encouraging, as it is considerably narrower than those we have flown previously.[13,15] We anticipate that the narrower trough may provide a corresponding improvement in radiation tolerance, and plan a particle irradiation campaign to test this conjecture. We discuss radiation tolerance in Sec. 3.2.

We see clear variation of CTI with temperature over the range we have explored: CTI increases by about a factor of two as temperature falls from −26°C to −58°C. We also find that serial CTI is lower than parallel CTI. This might be a consequence of the much higher transfer rate in the serial register, though the slightly higher clock amplitude applied to the serial register (4.0 versus 2.7 V, peak-to-peak) may also play some role. In any case, temperature and clock rate dependencies of CTI have been explored previously by many authors (e.g., Ref. 16 and references therein), and we return to this subject in our discussion of radiation tolerance in Sec. 3.2. We note that the charge injection register of the CCID93 allows us to investigate the mechanisms responsible for CTI in these devices in detail. We defer further discussion of this topic to a future work.

3 CCDs for Lynx: Concepts, Challenges, and Opportunities

3.1 *Lynx HDXI Focal Plane*

The HDXI field of view and spatial resolution requirements listed in Table 1 imply a ∼4096 × 4096 pixel focal plane with 16-μm pixels. Focal planes of this format and pixel size are readily available today. For example, the recently launched, Explorer-class Transiting Exoplanet Survey Satellite[17] features four visible-band cameras, each of which contains a four-CCD focal plane from MIT Lincoln Laboratory meeting these specifications.

Reading such an array at the rate required for HDXI (100 $\mathrm{frames\,s^{-1}}$) generates 1.6 $\mathrm{Gpixels\,s^{-1}}$. Assuming a pixel rate of 5 MHz per amplifier, a minimum of ∼350 amplifiers must operate in parallel to provide the required throughput. A four-chip array of 2048 × 2048 pixel frame-transfer CCDs, each with 128 amplifiers, could meet this requirement. Devices with as many as 128 parallel outputs have been produced at MIT Lincoln Laboratory, though more efficient output buffer/drivers than the discrete JFET die in current use would likely be required to maintain the acceptable power dissipation on the (cooled) focal plane.

The curved optimum focal surface of the Lynx mirror assembly introduces a significant complication. In fact, the radius of curvature of this surface varies strongly with x-ray energy, and an "optimum" surface can in principle only be defined for a particular source spectrum and a specific set of angular resolution criteria. This optimization has not yet been completed for Lynx. For purposes of this discussion, we assume that the optimum surface has a radius of 2.1 m, which is close to the optimum value to maximize subarcsecond field of view for monochromatic sources emitting at 1 keV.

One approach to matching this surface, adopted in the current Lynx design reference mission for the HDXI, is to approximate it by tiling a relatively large number of four-side abuttable chips (21 are specified in the DRM HDXI), each of 1024 × 1024 pixels. In this configuration, a frame-transfer architecture would be problematic, and a segmented CCD architecture, analogous to that used in the 60-chip Pan-STARRs[18] focal plane, may be appropriate for the HDXI. Each Pan-STARRs device is actually an 8 × 8 matrix of segments, with each segment's pixel array served by its own output amplifier. The device is read via an 8:1 multiplexer that allows eight segments to be read simultaneously, whereas the remainder of the segments integrate on the sky. A notional segmented, 1k × 1k device for HDXI could be organized in 16 rectangular segments, each with 1024 × 64 pixels and 32 parallel outputs. On-chip 16:1 multiplexers would allow each segment to be read consecutively (i.e., with all 32 outputs operating simultaneously), while the other segments integrate on the sky.

An alternative, possibly simpler approach is to deploy curved detectors. In this case, only four 2048 × 2048-pixel detectors would be required, and the framestore architecture described

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above could be adopted. Spherically curved silicon detector technology has been demonstrated for both CMOS[19] and CCD[20] devices, in the latter case with detectors quite similar in size and other characteristics to those required for Lynx in a fielded, multichip focal plane. As shown in Ref. 20, at the curvature required for Lynx, the strain induced in the sensor would be quite modest (roughly two orders of magnitude below the fracture limit for silicon), and the corresponding change in band-gap (<1 meV) and dark current should thus be negligible. We also note that fabrication and packaging techniques for curved sensors are well-understood.

Both of these notional configurations appear to be capable of meeting the HDXI frame rate requirements with significant margin, given 5-MHz pixel output and charge transfer rates, though a comprehensive technology development program must be completed to validate this assertion. Our purpose here is not to present a comprehensive or definitive comparison, but we can note some salient differences. The framestore architecture is likely simpler from a sensor design and fabrication point of view in that it requires neither on-chip multiplexing nor accommodation for output amplifier wiring through the imaging array. It also requires many fewer (internal) amplifiers (512 versus 8192 total for the focal plane), and thus would probably allow more accurate calibration. (Note that either CCD configuration would entail fewer amplifiers, by a factor >1000, than conventional active pixel sensors; see Sec. 3.3). In addition, a four-detector focal surface would have smaller gaps and greater field of view fill-factor, and would likely offer savings in complexity and cost of design, fabrication, and test of the HDXI detector assembly. On the other hand, the segmented architecture features much shorter charge transfer distances, and thus inherently better radiation tolerance, and probably entails lower peak on-chip power dissipation. The choice between these alternatives will require joint consideration of mirror assembly and HDXI design characteristics.

3.2 *Radiation Tolerance*

It is well-known that CCD performance can be adversely affected by particle radiation encountered in space environments. Energetic particles can displace atoms in the silicon lattice and introduce defects into the bulk of the device. The resulting silicon interstitials and vacancies can travel and form associations with each other and impurity atoms, producing a variety of configurations and associated electron energy levels inside the bandgap. These localized electron states can trap electrons and release them at a later time, causing CCD CTI and degrading spectral resolution.

Over the years, our group and others have developed and demonstrated a variety of effective CCD radiation-hardening techniques and countermeasures, including the buried-channel trough implant,[21] precision charge injection,[22] judicious choice of operating temperature, and careful shielding. We expect that all of these measures would be implemented for Lynx CCDs. It is important to recognize, however, that radiation-induced CTI is determined by the relation between trap emission time and CCD clock periods. Given the much higher transfer rates required of a Lynx CCD, it is crucial to understand how the radiation tolerance of Lynx sensors might differ from those of slower devices. Moreover, since the relevant time scales also depend on device temperature, consideration of the physics of radiation damage is essential in determining detector temperature requirements for Lynx. Ultimately, of course, theoretical considerations must be confirmed by experiments. As noted in Sec. 2.6.2, we plan to conduct radiation tests as part of our current development program.

Here we review the species of defects in silicon and consider the range of trap emission times in conjunction with characteristic CCD clock transfer times. For purposes of this discussion, we assume the frame-transfer architecture described in Sec. 3.1, as this appears to be the more sensitive to particle radiation. Vacancies in the silicon lattice created by incident radiation are mobile even at low temperatures and can travel through the entire device. Reacting with each other they can form stable defects called divacancies (V–V). Vacancies can also form complexes with phosphorous (P–V centers) and oxygen (O–V centers) atoms; these are also important stable trap sites. Another radiation-induced defect can arise if a silicon interstitial atom interacts with carbon, a common impurity in silicon wafers. In this reaction, a substitutional C atom replaces a Si interstitial atom (becoming Ci). Ci, in turn, can form complexes with P atoms (Ci–P). Ci–P is a metastable electron trap with several energy levels; the harmful one for CCD performance lies 0.3 eV below the conduction band. This defect may be responsible for "reverse annealing" in which a device exhibits increased CTI when warmed after cold irradiation.[23] Emission times for these traps are shown as a function of temperature in Fig. 10, calculated from published energy levels and cross sections,[24–26] along with relevant charge-transfer time intervals.

If the emission time is shorter than relevant CCD charge-transfer times, then trapped charge will be released quickly enough to keep up with the rest of its packet and the defect will have little effect on performance. Conversely, traps with emission times longer than the typical period between passages of a charge packet through any pixel (roughly the frame time for the parallel register transfer of concern to Lynx) will stay filled and are therefore also effectively disabled. The lower horizontal line at 100 ns corresponds to the nominal 5-MHz parallel transfer rate: traps with much shorter time constants than this will not affect performance. The upper horizontal line is defined by the frame time (projected to be 10 ms). Traps with much longer time scales will tend to remain filled. Clearly, the effect of radiation damage will depend on CCD readout rate as well as on temperature.

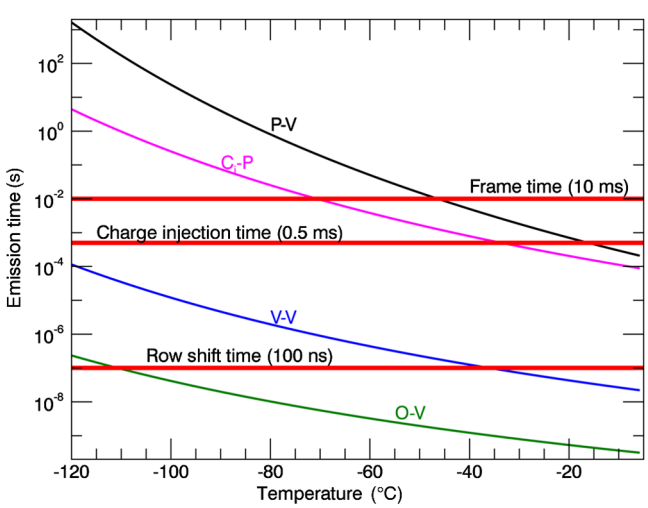

Fig. 10 Trap emission times for radiation-induced defects in silicon as a function of temperature. Horizontal red lines indicate typical transfer times envisioned for Lynx CCDs.

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The two slower phosphorus-related defects pose a problem at temperatures above −80°C. However, trapping effects in this regime can be reduced using controlled injection of charge to periodically fill these traps. This is illustrated by the "charge injection time" line in Fig. 8. A notional charge injection scheme for Lynx (injecting in one row of each 128) ensures that every trap is filled by injected charge at least every 0.5 ms, so that phosphorus-related defects are mitigated at temperatures below −40°C. This is crucial for our *n*-channel devices. This technique was implemented by our team on the Suzaku CCDs and proved to work extremely well in space, reducing the rate of CTI degradation by a factor of five.[27]

The O–V center is unimportant at temperatures above −80°C because this trap empties faster than any of the charge transfer rates. The remaining trap V–V lies in a time-constant regime where it will empty rapidly during image acquisition and thereby affect the CTI at the warmer temperatures. Here we rely on trough implants to minimize the number of divancies encountered by signal charge during readout. Studies in the early 1990s made it clear that radiation-induced CTI may be

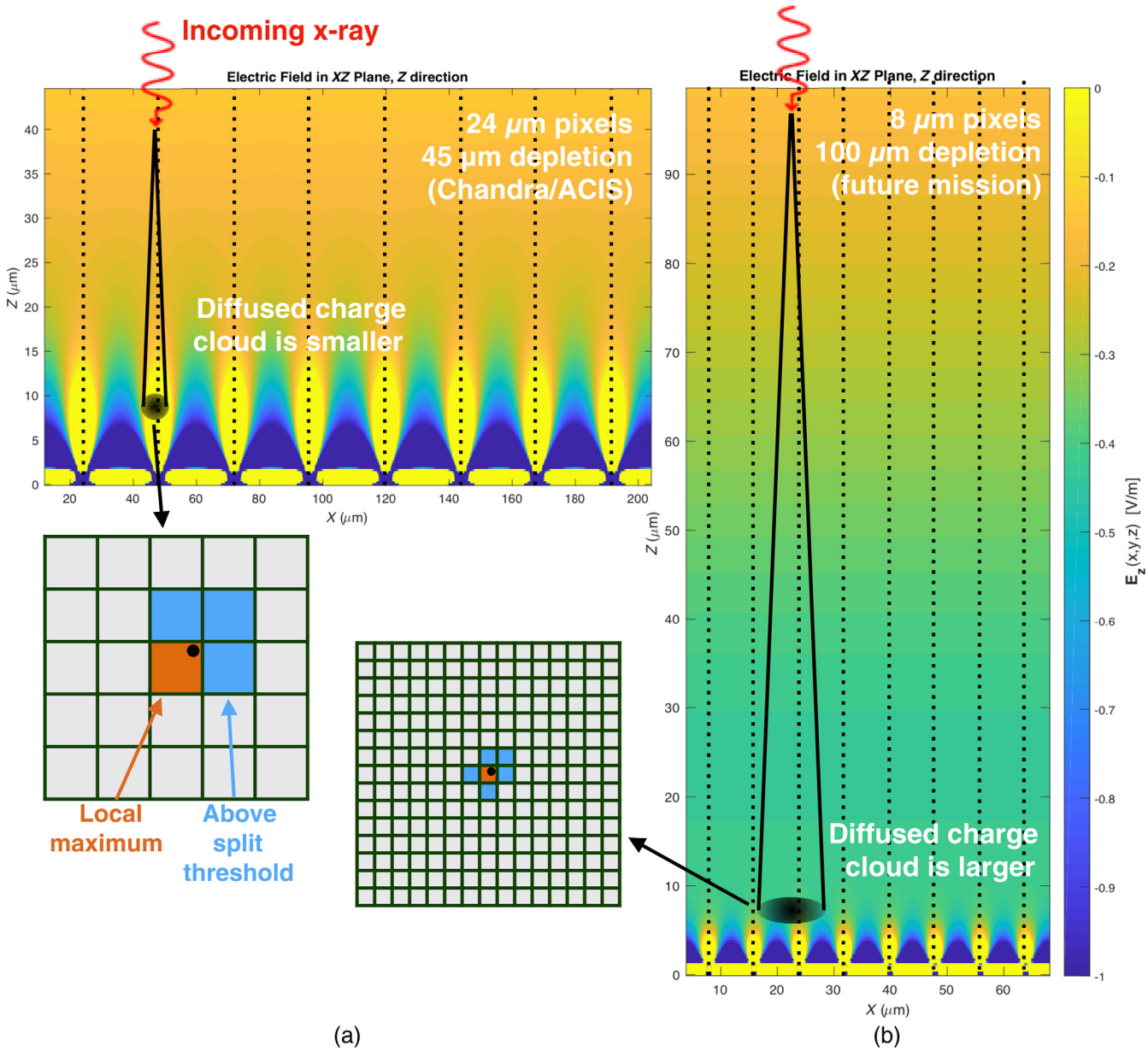

Fig. 11 Cross-section view of the vertical (*Z*-direction) electric field in two notional BI silicon detectors: (a) a 45-μm-thick device with 24-μm pixels similar to that used for Chandra/ACIS and (b) a 100-μm-thick device with 8-μm pixels that might be used on a future x-ray mission. Lynx HDXI requires pixels no larger than 16 μm and depletion depth of 100 μm. X-rays are shown schematically entering from the top and interacting within the depleted region at a depth dependent on energy. The charge cloud diffuses laterally as it travels quickly to the buried channel at the bottom. In the 24-μm pixel device, this spread is much smaller than a pixel, and so can only be distributed in four pixels in the worst case where it falls on a corner, as shown in the grid representing pixel values produced by the event; the black dot is the center of the charge cloud. In the thicker, smaller pixel device, the spread is similar to the pixel size, resulting in more multipixel events and events spreading to more than four pixels.

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reduced with narrower troughs. The results we presented in Sec. 2.6.2 show that troughs 2.5× narrower than those of the successful Chandra and Suzaku devices can now be fabricated, suggesting the possibility of significant further improvement in radiation tolerance.

Our flight experience with Chandra and Suzaku CCDs and an assessment of the relevant radiation environments lead to an estimate of radiation effects on Lynx CCDs. Assuming four-chip, $2k \times 2k$ pixel framestore detector configuration (the case demanding the greatest radiation tolerance), detector temperature between −60°C and −80°C, shielding comparable to Chandra/ACIS (∼10 $gm\,cm^{-2}$ Al), charge injection and a (conservative) 1-μm-wide trough, we expect a CTI degradation rate about a factor of 3 to 4 less than observed on Suzaku. This implies a gain nonuniformity increase across the Lynx focal plane of 0.5% to 0.7% per year at 5.9 keV. This change could be calibrated, as it was for Suzaku, to about 0.1%. The worst-case change in spectral resolution is an increase in FWHM at 5.9 keV of 2.5% (3 eV) per year, i.e., FWHM rising from 130 to 145 eV by the end of a nominal 5-year mission. We regard this modest effect as acceptable for Lynx. For the segmented detector architecture, radiation tolerance would nominally be better by a factor of 64. We plan measurements to test the assumptions underlying these estimates.

3.3 *Charge Collection*

A unique challenge posed by Lynx to both CCD and APS sensor technology is the requirement for relatively small (16 μm) pixels with relatively large (∼100 μm) depletion depth. In this configuration, charge packets produced by photoelectrically absorbed x-rays must generally drift a significant distance before they are collected in a pixel, which in turn allows significant lateral diffusion. A consequence is that for a very large fraction of x-ray events detected by the HDXI, the signal charge will be shared among several pixels, as shown schematically in Fig. 11. The charge in each of these pixels must be measured accurately and summed to meet Lynx performance goals, and typically a threshold is enforced to prevent noise outliers from contaminating the energy reconstruction. Charge split below this threshold leads to (1) a loss of QE at low energies as split events are lost below the threshold and (2) a loss of knowledge of the x-ray photon energy, as split events are incompletely reconstructed with a continuum of lower energies compared to the true value. Minimizing these issues imposes demanding requirements on detector noise and pixel-to-pixel response uniformity.

To understand the subtle trade-offs in pixel size, depletion depth, detector noise, and broad-band x-ray response, we performed simulations of charge diffusion and event reconstruction in detectors with properties similar to those of a notional Lynx detector. These results are described in detail in a separate work,[28] and here we provide a summary. We emphasize that although we assume the detector is a CCD, the results are independent of the readout method of the detector and are applicable to silicon-based CMOS or other APS devices. We start with three-dimensional calculations of the internal electric field in the detector, obtained from a semiconductor simulator for silicon CCDs, POISSON_CCD.[29] Photons of different energies interact in the CCD at depths drawn from the attenuation function, and the charge cloud produced diffuses as it is drawn to the gate structure, as determined by the electric field distribution. We note that our approach involves a number of simplifications. For example, it ignores the electrostatic interaction of free electrons and holes during the charge collection process. Estimates by the author of POISSON_CCD (C. Lage, private communication) suggest that these effects may lead to a net increase in the final electron cloud size by order of 10%. Our results should thus be regarded as a first approximation to the impact of charge spreading on device performance. More detailed analysis will be warranted as detector designs mature.

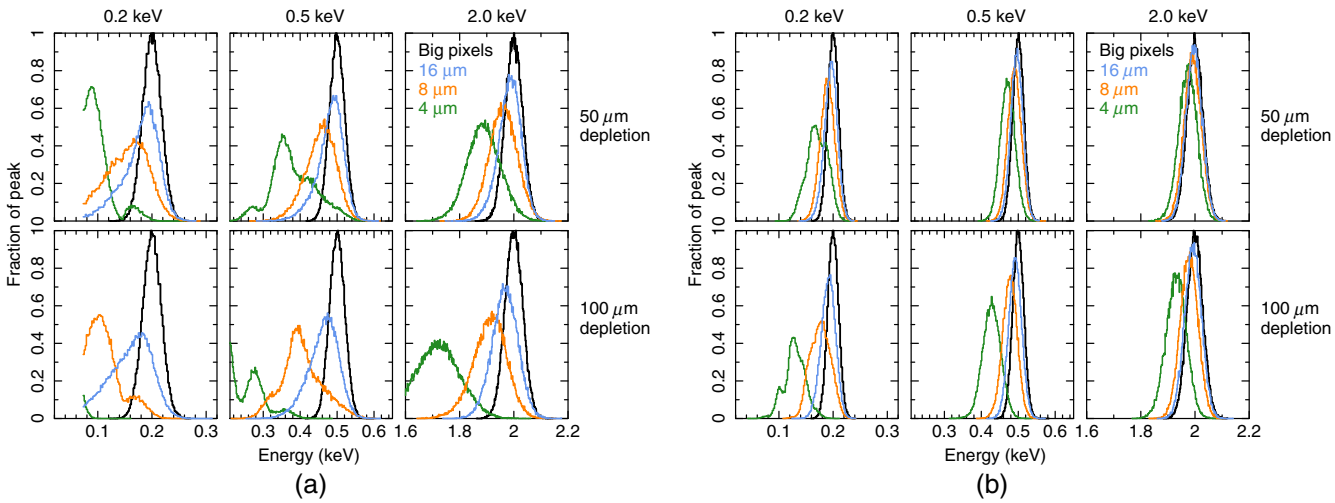

Fig. 12 Response to monochromatic photons of three energies for (a) $4e^-$ and (b) $1e^-$ readout noise, for depletion depths of 50 and 100 μm. Black curves ("big pixels") are for infinitely large pixels, i.e., assuming all charge is collected by one pixel; other colors are for different pixel sizes. The same number of input photons was used for each histogram, and all were normalized by the peak of the "big pixels" histogram. Not only the center and width of the response changes with pixel size, but the shape and mode as well, indicating that both QE and the knowledge of the reconstructed energy seriously degrade with smaller pixels and larger depletion depth in the presence of moderate pixel-based noise. Reducing the readout noise greatly improves the energy reconstruction at soft energies, except for smallest pixels and largest depletion depth.

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To the charge collected in each pixel, we add readout noise and then identify and reconstruct the events according to standard procedures used in previous missions. In particular, to ensure that <1% of evenly split four-pixel events are lost, we require at least one pixel with $(E_{\min}/4) - 3\sigma_{\mathrm{ro}}$, where $E_{\min}$ is the minimum energy of interest and σ_{ro} is the RMS readout noise, both in the same units of e^- or energy. This minimum is the event threshold. Neighboring pixels above the split threshold of 5σ are included in the event energy summation.

Photons with energy <1 keV all interact very close to the backside entrance window, and therefore, as an ensemble suffer the greatest lateral diffusion during charge collection. As we show in Figs. 12 and 13, a combination of small pixels, deep depletion, and high readout noise conspire to drop the signal in neighbor pixels of a given event below the split threshold, producing a low summed event energy for such photons. The combined response to the ensemble of monoenergetic photons in this case is non-Gaussian with a large variance, and this renders reconstruction of the incoming energy distribution difficult. Readout noise has the greatest effect on the soft x-ray response of a detector like the notional HDXI; reducing the readout noise from 4 to $1e^-$ greatly improves the knowledge of the ensemble of incoming photon energies, especially for small pixels where several pixels are involved in each event reconstruction. Pixels of 8 and 16 μm produce adequate energy reconstruction at the full range of depletion depth and energy for $1e^-$ readout noise. For the HDXI readout noise requirement of $4e^-$, 8-μm pixels result in many multipixel events that greatly degrade the response at soft energies (orange curves in Fig. 12 left, bottom panels). This is one important reason to adopt the largest pixel size consistent with angular resolution requirements (16 μm for the Lynx HDXI). Indeed, Fig. 13(b) shows that the HDXI requirement for low-energy spectral resolution (70 eV, FWHM; see Table 1) is unlikely to be met by any silicon detector technology unless read noise significantly <4 electrons, RMS can be achieved. We expect that more detailed simulations accounting for the effects of electrostatic repulsion within the charge cloud will strengthen this conclusion.

Lateral charge diffusion provides benefits as well as challenges for high-spatial-resolution missions such as Lynx. In particular, the charge diffusion discussed above can be exploited to provide subpixel positioning of detected photons to exquisite precision with even moderately sized pixels such as those baselined for the HDXI.[30,31] The pixel size needed to sufficiently sample a particular PSF is a matter of current study. Our simulations can address this in a tunable way, and we will include subpixel positioning to optimize pixel size as part of our future work.

It should finally be noted that, for active pixel sensor or other detector technologies which employ separate amplifiers in each pixel, the gains of the amplifiers in adjacent pixels must be calibrated with a relative accuracy comparable to or better than the spectral resolving power ($\delta E/E$) required. This is particularly important for instruments such as the Lynx HXDI, where the majority of x-ray events are expected to be multipixel for the reasons described above. For the HDXI at 6 keV, for example, $\delta E/E = 2\%$ FWHM is specified, implying that pixel-to-pixel gain nonuniformity of better than 1% RMS is required for optimal spectral resolution. A potential virtue of the DCCD approach, with its relatively small number of amplifiers relative to conventional active pixel sensors, is a more accurate calibration and thus better spectral resolution.

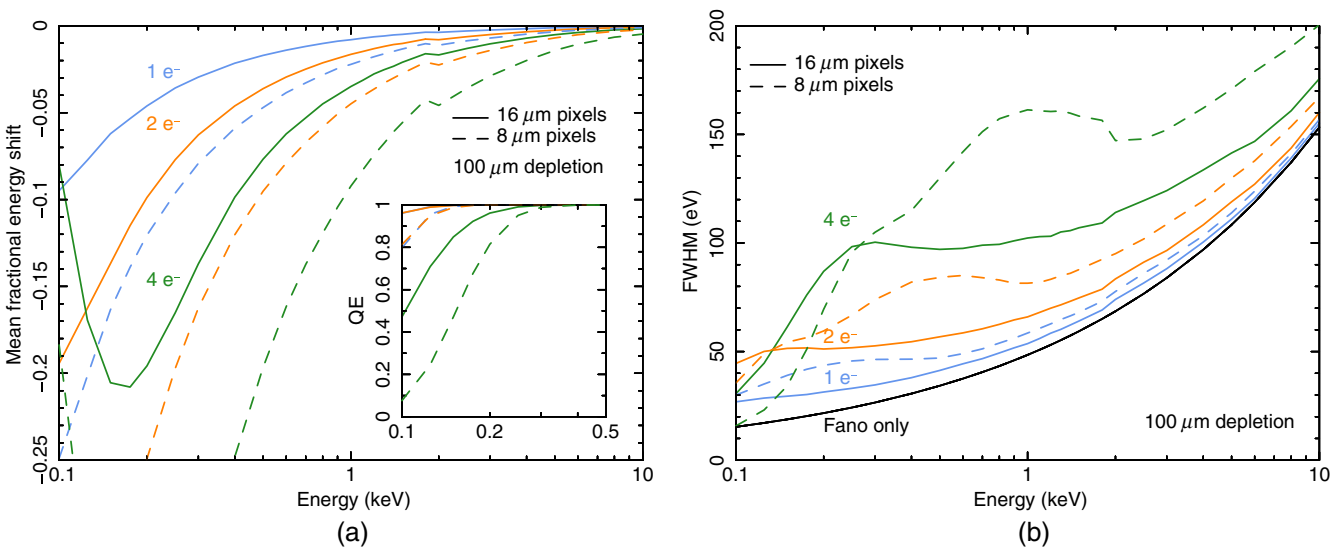

Fig. 13 (a) Fractional energy (gain) shifts as a function of energy for simulated photons in a 100-μm-thick detector. Smaller pixels produce substantial shifts at all energies and for all levels of readout noise and are likely to produce lost events at the softest energies. Note that the upturn below 0.2 keV for $4e^-$ readout noise is an artifact of the event threshold; since events cannot have energies below 0.1 keV, the mean energy offset approaches zero near this limit. The inset shows the relative QE reduction due to events lost below this threshold, which is significant for $4e^-$ readout noise. (b) Spectral response width (FWHM) as a function of energy for simulated photons in a 100-μm detector. Small pixels result in poor response at soft energies except at the lowest readout noise. The drop in FWHM at low energies for $4e^-$ readout noise is an artifact of fitting a single Gaussian to the multimodal structure in the histograms shown in Fig. 12, lower panels.

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4 Summary and Plans

We have characterized x-ray CCD detectors operating with CMOS-compatible clock amplitudes at pixel rates from 1.25 to 5 MHz and parallel transfer rates as high as 1 MHz. These rates are 50 and 100 times faster, respectively, than those operating now on Chandra and have been achieved while consuming comparable clock power per unit area. Read noise as low as 4.6 electrons RMS at 2.5 MHz has been measured for our latest CCID93 detector and single-pixel-event x-ray spectral resolution is better than 150-eV FWHM at 5.9 keV. We believe these results demonstrate that CCDs are a credible sensor technology for the Lynx HDXI and XGS instruments.

We measure CTI $<10^{-5}$ per pixel transfer at parallel register transfer rates up to 1 MHz and clock amplitudes as low as 1-V peak-to-peak. We find that buried channel trough implants as narrow as 0.8 μm improve charge transfer performance. Our test devices exhibit a significant increase in CTI as temperature decreases from −26°C to −58°C.

We have discussed two detector array concepts potentially relevant for Lynx and noted the potential value of curved detectors for simplifying the Lynx HDXI focal plane configuration. We considered the likely effects of radiation damage on CCDs operating at rates required for the HDXI. Radiation hardening measures demonstrated in previous flight missions appear to be capable of providing adequate radiation tolerance.

The small pixels (one-quarter of the area of those required for Lynx instruments) and relatively deep depletion of our front-illuminated test devices have allowed us to study the effect of interpixel charge-sharing on spectral resolution. We infer that charge-sharing significantly broadens the single-pixel-event spectral response we observe at 5.9 keV. We note that the Lynx HDXI requirements for back-illuminated detectors with small pixels and large depletion regions similarly imply that charge-sharing will have significant effects on spectral resolution and low-energy detection efficiency. Our simulations of these effects imply that read noise levels even lower than those currently specified for HDXI sensors will be required to meet spectral resolution requirements. This conclusion holds for any silicon detector technology adopted for Lynx HDXI.

We expect to make further progress developing CCD technology for Lynx in the near future. Lincoln Laboratory detectors with amplifiers very similar to those we report on here have demonstrated significantly lower-noise-levels (<3 electrons RMS) at comparable rates, and we are experimenting with an alternative, high-responsivity (SiSeRO) amplifier architecture that may exhibit even lower noise. The charge injection capabilities built into our current test sensor will allow us to conduct detailed studies of the mechanisms responsible for the observed CTI. A back-illuminated version of the CCID93 is currently in fabrication and will be available for test in a few months. We will use it to explore the soft x-ray response to energies as low as 0.3 keV. A radiation test program on these devices will be carried in the coming year. Completion of these NASA-funded Strategic Astrophysics Technology studies will provide the groundwork needed to design a CCD that meets Lynx requirements for frame rate, x-ray performance, and radiation tolerance.

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